

## REMARKS

Claims 1-24 are pending in the present application. Applicant respectfully submits that the application is allowable without amendment

Claims 1-8 and 10-19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Lakhani, *et al.* (U.S. Patent Application Publication No. 2003/0126385) in view of SanDisk Secure Digital Card product manual, version 1.9 (hereinafter "SD manual"). Other dependent claims have been rejected over of these references in combination with additional prior art. Applicant respectfully traverses these rejections.

Claim 1, as previously presented, specifically recites "using the one or more unused bits of the address argument of the command as an addressing mode field to determine whether said address argument is a byte address argument or a block address argument, wherein the remaining bits provide a byte address when the address argument is a byte address argument and the remaining bits provide a block address when the address argument is a block address argument." Applicant respectfully submits that neither Lakhani nor the SD manual, either alone or in combination, ever teach a byte addressing mode, much less a command that provides an addressing mode field and an address argument as required by claim 1.

The Office Action cites the bits C1 and C2 as being "used as a first mode/byte addressing mode." This conclusion is factually inaccurate. Lakhani never teaches or suggests any transaction in byte address mode – all modes provide block addresses. Referring to Table A (Par. 73), Lakhani teaches the modes as controlled by C1 and C2:

C1C2 = 00 – first mode where XC(7:0) set to "single erase block selection bits" (Par. 75)

C1C2 = 1X – second mode where XC(7:0) set to "block selection bits E(7:0)" (Par. 76)

C1C2 = 01 – third mode where XC(7:0) set to "multiblock selection bits" (Par. 77).

In each case, Lakhani operates in a block addressing mode. In the first case, a single block is accessed; in the latter cases multiple blocks are accessed. The Examiner has not shown, nor can Applicant find, any example where Lakhani has an argument that provides a byte address.

Further, the SD manual does not overcome this shortcoming. In particular, the SD manual never teaches a command that includes an addressing mode field to determine whether the address argument is a byte address argument or a block address argument. This is clear from the commands taught starting on page 4-17 of the SD manual. (Since the Office Action includes only selected pages of the manual, Applicant has provided the entire manual so that the record can be clear as to what the SD manual does and does not teach.) Referring to page 4-21, the SD manual teaches Block Read Command and Block Write Commands. The manual never teaches or suggest a command that includes a byte address argument.

Applicant notes that the SD manual teaches that a block can be a single byte. The manual, however, never teaches a command that includes an addressing mode field to determine whether the address argument is a byte address argument or a block address argument. Rather the manual teaches a separate block length command (CMD16 shown in Table 4-4 on page 4-21). The read, write and erase commands are all block command and do not include any mode field to alter this.

Applicant, therefore, respectfully submits that claim 1 is allowable over the references of record.

Claims 2-7 depend from claim 1 and add further limitations. It is respectfully submitted that these claims are allowable over the references of record in view of their dependence on an allowable claim as well as the additional limitations.

Claim 8, as previously presented, specifically recites "a controller adapted to use one or more bits of a command as an addressing mode field to determine whether an addressing mode to access said memory unit is a byte addressing mode or a block addressing mode and to send a command to access data within said memory unit according to said addressing mode." As discussed above with reference to claim 1, the prior art cited in the rejection never teaches or suggests a byte addressing mode, much less an addressing mode field to determine whether the addressing mode is a byte addressing mode or a block addressing mode. It is therefore respectfully submitted that claim 8 is allowable over the references of record.

Claims 9, 10 and 17 depend from claim 8 and add further limitations. It is respectfully submitted that these claims are allowable over the references of record in view of their dependence on an allowable claim as well as the additional limitations.

Claims 11 and 12, as previously presented, both recite "a controller to determine whether an addressing mode to access said memory unit is a byte addressing mode or a block addressing mode and to send a command to access data within said memory unit according to said addressing mode." As discussed above with reference to claim 1, the prior art cited in the rejection never teaches or suggests a byte addressing mode.

Further claim 11 recites that "the addressing mode is associated with the ninth bit of a 48-bit command having a 32-bit address argument" and claim 12 recites that "the addressing mode is associated with the 40-th bit of a 48-bit command having a 32-bit address argument." Nothing in the prior art teaches or suggest this specific configuration.

Claim 13, as previously presented, specifically recites "using one or more bits of a command as an addressing mode field to determine whether an address argument of the command is a byte address argument or a block address argument." As discussed above with

reference to claim 1, the prior art cited in the rejection never teaches or suggests a byte addressing mode, much less an addressing mode field to determine whether an address argument of the command is a byte address argument or a block address argument. It is therefore respectfully submitted that claim 13 is allowable over the references of record.

Claims 14-16 depend from claim 13 and add further limitations. It is respectfully submitted that these claims are allowable over the references of record in view of their dependence on an allowable claim as well as the additional limitations.

Claim 18, as previously presented, specifically recites "receiving a command that includes an address argument comprising a plurality of address bits and an addressing mode field, the addressing mode field indicating whether the address argument contains a byte address or a block address, the block address and the byte address having the same number of bits." As discussed above with reference to claim 1, the prior art cited in the rejection never teaches or suggests an addressing mode field indicating whether the address argument contains a byte address or a block address. It is therefore respectfully submitted that claim 13 is allowable over the references of record.

Claims 19-24 depend from claim 18 and add further limitations. It is respectfully submitted that these claims are allowable over the references of record in view of their dependence on an allowable claim as well as the additional limitations.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Ira S. Matsil, Applicant's attorney, at 972-732-1001, so that such issues may be resolved as expeditiously as possible. The Commissioner is hereby authorized to charge any fees that are due, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,



Ira S. Matsil  
Attorney for Applicant  
Reg. No. 35,272

Date: 8/29/08  
SLATER & MATSIL, L.L.P.  
17950 Preston Rd., Suite 1000  
Dallas, Texas 75252  
Tel.: 972-732-1001  
Fax: 972-732-9218